REMARKS

This amendment responds to the Office Action dated November 26, 2008, in which the Examiner rejected claims 1-22 under 35 U.S.C. § 103.

Applicant would like to thank the Examiner for acknowledgement of the priority papers. However, Applicant respectfully points out that box 12a 3 should be indicated rather than box 12a 1 on the Office Action summary PTOL-326.

As indicated above, claims 1 and 12 have been amended in order to make explicit what is implicit in the claims. The amendments are unrelated to a statutory requirement for patentability.

Claim 1 claims an interleaving device and claim 12 claims an interleaving method. The device and method include a first interleaving means/step performing folding interleaving on first data comprised of plural input packets, in units of a data word or plural consecutive data words. A second interleaving means/step performs interleaving, in units of a packet, on second data directly output/generated by the first interleaving means/step. The second data is comprised of plural packets.

By performing interleaving on second data directly output/generated by a first interleaving means/step as claimed in claims 1 and 12, claimed invention provides an interleaving device and method which can correct a significant burst error using an error correction code having a small code length. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 12.

Claims 1-22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Sako* (U.S. Patent No. 5,732,088) in view of *Higashida, et al.* (U.S. Patent No. 6,826,181).

Sako appears to disclose in FIG. 1 interleavers 3a or 3b change the data symbols or the code sequence of the parity generated by the C2 encoder (Col. 5, lines 17-19). The two interleavers 3a and 3b are provided for selecting the interleave length corresponding to the record density of the optical disk 20 (Col. 5, lines 60-62). The interleaver 3a is selected when the optical disk 20 is a standard record density type optical disk. The interleaver 3b is selected when the optical disk is a high density optical disk (Col. 6, lines 18-22). FIG. 6 shows an error-correction encoding process in which data is recorded on a standard density type optical disk. Input symbols are supplied to a C1 encoder 105. The output is supplied to a C2 encoder 102 through a delay circuit group 103a for the interleaving process. The C2 encoder 102 generates a C2 parity Q of 14 bytes with a Reed-Solomon Code. The C1 encoder 105 encodes not only data, but the C2 parity of the C1 code. Thus, the C2 parity Q is fed back from the C2 encoder 102 to the C1 encoder 105 through the delay circuit group 107a for the interleaving process. The delay circuit groups 103a and 107a compose the interleavers for the standard density type optical disk (Col. 9, lines 15-35).

Thus, *Sako* merely discloses in FIG. 1 interleavers 3a, 3b. However, the output from interleaver 3a in *Sako* is <u>not</u> directly input to interleaver 3b. Therefore, nothing in *Sako* shows, teaches or suggests a second interleaving means that directly receives output from a first interleaving means as claimed in claim 1, or a second interleaving step of performing interleaving on second data directly generated by a first interleaving step as claimed in claim 12. Rather, *Sako* teaches away from the claimed invention since the output from interleavers 3a, 3b are selectively output to C1 encoder 5.

Higashida, et al. appears to disclose in FIGS. 21, 26, 29 and 36, a first interleaving processing means for executing a first interleaving process by writing a data string into a first storage apparatus having a first matrix form in a first direction and thereafter reading from the first storage apparatus the data in a second direction perpendicular to the first direction and outputting the data after the first interleave process in a unit of data in the second direction. A second parity adding means adds a predetermined parity to data output from the first interleave processing means and outputs the data. A second interleave processing means executes a second interleave process by writing the data output from the second parity adding means into a second storage apparatus having a second matrix form in a fourth direction of the second matrix coinciding with the second direction of the first matrix and thereafter reading from the second storage apparatus the data in a third direction perpendicular to the fourth direction of the second matrix and outputting the data obtained after the second interleave process in a unit of data in the third direction (Col. 4, lines 24-55).

Thus, *Higashida, et al.* merely discloses a second interleave processing means executing a second interleave process on data output from a parity adding means. Nothing in *Higashida, et al.* shows, teaches or suggests (a) a second interleaving means directly receiving output from a first interleaving means as claimed in claim 1, or (b) a second interleaving step of performing interleaving on second data directly generated by a first interleaving step as claimed in claim 12. Rather, *Higashida, et al.* merely discloses that the second interleaving means executes an interleave process on data output from a parity adding means.

Furthermore, *Higashida, et al.* merely discloses that the data output from the second interleaving means is output in a unit of data in a third direction. Thus, nothing in *Higashida, et al.* shows, teaches or suggests (a) a first interleaving in units of a data word or plural consecutive data words, and (b) second interleaving in units of a packet as claimed in claims 1 and 12. Rather, *Higashida, et al.* merely discloses after a first interleave process outputting data of a unit of a second direction and after a second interleave process outputting data of a unit of data in a third direction.

The combination of *Sako* and *Higashida, et al.* would not be possible since the interleavers 3a and 3b of *Sako* separately output data into an encoder, whereas *Higashida, et al.* outputs interleave data to a parity adding circuit. Even assuming arguendo that the references could be combined, the combination would merely suggest that after selection of output from interleavers 3a and 3b by selecting unit as taught by *Sako*, to output the selected interleave data to a parity adding circuit as taught by *Higashida, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) a first interleave means performing folding interleaves in units of a data word or plural consecutive data words and a second interleave means directly receiving output from the first interleave means and performing interleaving in units of a packet as claimed in claim 1, or (b) a first interleaving step of performing folding interleave in units of a data word or plural consecutive data words and a second interleaving step of performing interleaving in units of a packet of second data directly generated by the first interleaving step as claimed in claim 12. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 12 under 35 U.S.C. § 103.

Claims 2-11 and 13-22 depend from claims 1 and 12 and recite additional features. Applicant respectfully submits that claims 2-11 and 13-22 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Sako* and *Higashida, et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2-11 and 13-22 under 35 U.S.C. § 103.

Thus it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 50-0320.

Respectfully submitted,

Frommer Lawrence & Haug LLP
Attorneys for Applicant

Date: February 10, 2009

By: _____
Ellen Marcie Emas
Reg. No. 32,131
(202) 292-1530